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10/565,551	09/11/2006	Ingrid M. Verbauwhede	UCLARF.003NP	2110

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
06/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/565,551	VERBAUWHEDE ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-11 and 14-20* is/are rejected.

7)☒ Claim(s) *3,4,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

The drawings are objected to because the supply line on Fig. 4B is not connected to transistor 405. Also, a solid dot should be placed on each of output nodes in Figs. 4B, 6, 9, and 10 in order to show which lines are being connected together. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 3, 4, and 12-14 are objected to because of the following informalities: Claims 14, line 3, the recitation, "ground" appears to be "supply voltage". Claims 3, 4, 12, and 13, line 3, the recitation, "open" appears to be "closed". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 5-11, and 14-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Tiri et al. ("A Dynamic and Differential CMOS Logic with Signal Independent Power Consumption to Withstand Differential Power Analysis on Smart Cards").

Regarding claim 1, Tiri discloses an apparatus comprising:

a sense amplifier based logic gate (see Fig. 4; see page 405) having an input network (DPDN), said input network comprising a differential pull-down network (DPDN; see page 404, section 2.1, first paragraph) wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network.

Regarding claim 2, Tiri discloses that wherein said differential pull down network comprises a special differential pull down network (DPDN; see page 404, section 2.1, first paragraph).

Regarding claim 5, Tiri discloses that wherein during evaluation a cross-coupled inverter (see Fig. 4 and 2.1 first paragraph) toggles to one state and provides a stable output when said differential pull-down network provides a path to ground.

Regarding claim 6, Tiri discloses a first transistor (M1 in Fig. 4; see page 404, section 2.1, second paragraph), which is always on, configured to prevent a floating node by serving as a path for sub-threshold currents.

Regarding claim 7, Tiri discloses differential output nodes (see page 404, section 2.1, second paragraph) configured to provide differential signals to a differential input.

Regarding claim 8, Tiri discloses that wherein said differential pull-down network is configured such that each node of said differential pull-down network both a first signal and an inverse of the first signal control a transistor that loads the node (see page 404, section 2.1, second paragraph).

Regarding claim 9, Tiri discloses a clocked transistor (see p-type transistors coupled to clk in Fig. 4) provided between output nodes of said logic gate such that when a clock-signal becomes low, said clocked transistor provides charge stored at one output node to partially charge said output nodes and said internal nodes to an intermediate voltage (see page 404, section 2.1, second paragraph).

Claims 10, 11, and 14-18 are similarly rejected as claims 1, 2, and 5-9 since Tiri discloses on page 404, section 2.1, third paragraph that "a generic p-gate is implemented as a gate that pre-charges to GND when clk is high and evaluates one node to VDD through a DPUN when clk is low. See Fig. 10 of present invention for inherent drawing for the above statement.

Regarding claim 19, the structure of Tiri (Fig. 4) inherently discloses a method for transforming a differential pull-down network for a logical function (AND/NAND), comprising:

identifying two expressions x and y that combine to the logical function according to a logical AND operation (see left branch of Fig. 4), x.y corresponding to a network x and a network y;

complementing the expressions in x and y to obtain the dual expression of the logical function, as a logical OR operation (see right branch of Fig. 4), /x + /y ;

transforming the OR operation into a transformed network /x • y + /y, providing the transformed network to an internal node of the x.y network and sharing the network y between the two branches x • y (left branch of Fig. 4) and /x • y + /y (right branch of Fig. 4); and

repeating the actions of identifying, complementing and transforming.

Claim 20, is similarly rejected as claim 19 since the structure of Tiri (Fig. 4) inherently discloses a method for transforming a differential pull-down network for a logical function, since a two-input AND/NAND operation is equivalent to a NOR/OR operation carried out on inverted input signals.

Allowable Subject Matter

Claims 3, 4, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and correct the claim objections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel D. Chang
Primary Examiner
Art Unit 2819

DANIEL CHANG
PRIMARY EXAMINER